Co Liner for Enhancement of Cu Damascene Interconnections

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Cu based interconnects have been widely used in advanced large-scale integrated circuits because of their resistance to electromigration and low resistivity, and they are formed by electrochemical deposition(ECD) after Cu seed deposition following barrier deposition on trench/Via. Introducing of copper barrier/seed (CuBS) enables continued high-performance interconnect scaling. In this study, for the integrated dual damascene hardware of 10nm node dimensions, we investigated the mechanism for Co liner enhancement of Cu gap-fill through wetting improvement of the PVD Cu seed. We evaluated the Cu reflow property using Magnetic-Field-Assisted Ionized Sputtering (MFIS) technique. Incorporation of oxygen and carbon in the CVD Co films (by AES and SIMS) depended on underlying materials, such as Ta, TaN, Copper film texture (by XRD) and agglomeration resistance (by AFM) showed correlations with amounts of in-film oxygen/carbon. The smallest roughness value due to the wettability was increased by the Co thin film. The pattern wiggling phenomenon caused by thermal expansion coefficient was relaxed when the TaN/Co/Cu multilayers have the tensile tendency. CVD Co liners are of interest for back end of the line (BEOL) interconnects due to improved Cu interconnect gap fill, especially at narrow feature widths. The above solutions may then enable CVD-Co/Cu seed integration as good candidate for liner material in the next generation technology with 10nm node extendibility.