Magnetron sputtering system design for TSV(through silicon via) applications

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Increasing stack density in semiconductor memory devices is leading the magnetron sputtering technology together with large area flat panel display industries (LCD, OLED). 3D stacking of each wafers inevitably includes vertical interconnection through metal plugs. Etching, liner deposition and final electroplating are the major steps. Very high vertical aspect ratio over 10 : 1 is required. Sputtered particles from the magnetron target surface is mostry neutrals and they cannot be easily controlled. The only available parameter knob is gas pressure. Low pressure sputtering was adopted with honeycomb shaped collimator to get rid of off-angled particles. As the opening size of the holes is reduced, more tight control of incoming angle distribution is required. Ionization and biasing of the wafers are the next solutions. Additional supply of energy to the electrons was realized either by rf coupling, e.g. inductively coupled plasma or by overpowering of the magnetron cathode (self ionized sputtering mode). In this presentation, review of high ionization magnetron sputtering system design will be done by numercal modeling as well as experimental works. ICP assisted magnetron sputtering, High Power Impulse Magnetron sputtering, Modulated Pulsed Power sputtering and magnetic field assisted self ionization sputtering are the major subjects to review. CFD-ACE+(ESI corp) is used in many areas of the numerical review: magnetic field calculation, cooling water flow dynamic calculation, heat transfer to the target and stress analysis. Simpified, but very useful homemade code was used in interpreting the electron trajectories in conjunction with major collisions with netrals to produce electrons and ions for maintaining magnetron plasmas.

This research was supported by a grant from the Reinforcemet of New development power in Equipments Project R&D Program funded by the Ministry of Trade, Industry and Energy, Republic of Korea with contract number (10067481)