Frontiers of industrial application of atomic layer etching

Alok Ranjan¹ and Peter Ventzek² ¹TEL Technology Center, America, LLC, U.S.A. ²Tokyo Electron America, Inc., U.S.A.

With shrinking critical dimensions, dry etch faces more andmore challenges. Minimizing each of aspect ratio dependent etching (ARDE), bowing, undercut, selectivity, and within die uniformly across a wafer are metby trading off one requirement against another. The problem of trade-offs isespecially critical for 10nm and beyond technology. At the root of the problemis that roles radical flux, ion flux and ion energy play may be both good andbad. Increasing one parameter helps meeting one requirement but hinders meeting the other. Self-limiting processes like atomiclayer etching (ALE) promise a way to escape the problem of balancingtrade-offs. ALE was realized in the mid-1990s but the industrial implementationdid not occur due to inherent slowness and precision loss from improper balanceof self-limiting passivation and its removal processes. In recent years, interest in ALE has revived and strides have been made by etch equipmentmanufacturers primarily through temporal, spatial or combination of these twopulsing approaches. Moderate success has been reported with some of thetrade-offs purported to be managed. Difficulty meeting requirements is due to theinability of plasma technologies to control ion energy at low and precisevalues. In this presentation, we demonstrate that ALE can achieve zero ARDE and infinite selectivity with ability to control profile. Experimental results willhighlight that careful consideration of surface process physics is required toachieve ALE and not simply "slow etching". ALE using three approaches for radical adsorption (1. chemisorption, 2.polymer deposition and 3. surface modification) and desorption using 3approaches (1. ion bombardment 2. substrate heating and 3. Chemical removal ofmodified layer) will be addressed with insights to solve critical problemsassociated to Si (Gate, Fin), SiO2 (Self-Aligned Contact), SiN (Gate Spacer, SIT spacer) etch.