The Enhancement of the Flash Memory Boosting Efficiency by Adding Deep N- Phosphorous Implantation

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The disturbance of the inhibitcells on the program operation should be minimized for decreasing the range ofeach state on NAND flash device. Rising the boosting potential on the programoperation, the difference between threshold voltage of program and erase cellscan be maximized. Decreasing the channel doping makes the boosting potentialrise. It can, however, result in a short channel effect because of theshrinking design rule.

The way of reducing depletioncapacitance is the compensation of Si substrate doping concentration throughthe N- phosphorous high energy implantation on the p-type substrate. The dopingcompensation widens the depletion area, and it makes the depletion capacitancedecrease. Since the boosting efficiencyimprovement on simulation can be converted to channel implantation dose down,the channel dose down by 0.9e+13 is as worthy as adding 90keV 7.0e+12cm^{-2}N- phosphorous implantation on the body.

The Vpass window margin has been reduced by 30% as the device shrank. The narrowVpass window led to performance degradations such as the endurance failureoccurred by the program disturbance of the erase cells during program-eraseoperation cycles. The local self boosting is used to improve the programdisturbance. The channel doping concentration needs to be decreased forincreasing boosting potential but the short channel effect gets worse at lowchannel doping concentration. In this paper, we discussed how to optimizesubstrate doping concentration of the NAND flash device to improve boostingefficiency by adding N- phosphorus high energy implantation on the p-typesubstrate.