Etching Characteristics of SiON Thin Films in CF_4+CHF_3+O_2 Inductively Coupled Plasma

Jihun Kim [1], Junmyung Lee [1], and Kwang-Ho Kwon [1]

[1]*Korea Univ., Korea, Republic of*

The resistance-capacitance delay of the signal becomes a critical issue in nano-semiconductors device fabricate process. It is the best to use low-k materials to reduce the delay [1]. The IMD (Inter Metal Dielectric) plays a key role as mentioned above, and mainly low dielectric materials are used to lower the capacitance among which SiON is a promising material. The research using CHF_3+CO and C_2F_6 plasma has been published [2-3], but the study of SiON etching process using CF_4+CHF_3+O_2 plasma has not been carried out to date. As the semiconductor device becomes more integrated, it is necessary to control the IMD materials more precisely in etching process. Therefore, in this study, the etching characteristics of SiON, which mainly used as the IMD in CF_4 + CHF_3 + O_2 inductively coupled plasma and the selectivity for Si, SiO_2 and PMMA were investigated. The etch rate of SiON, Si, SiO_2, and PMMA was measured by surface profiler (Alpha-Step). In addition, the etch profile was observed by a Scanning Electron Microscope (SEM). Furthermore, we used not only Double Langmuir probe (DLP) and Optical Emission Spectroscopy (OES) for plasma diagnostics but also X-ray Photoelectron Spectroscopy (XPS) to analyze surface chemical bonding state. Through the 0-dimensional modeling of CF_4+CHF_3+O_2 gas plasma, we will discuss the etching mechanism of the SiON films in detail and extract the optimal etching condition for both the high etching rate and selectivity. Finally, the performance of the IMD material will be evaluated by evaluating electrical characteristics such as I-V curve and C-V curve. After the plasma etching process, the research of sidewall damage is important, but currently study is insufficient. Therefore, we measured side wall damage using the e-beam lithography and chemical mechanical polishing techniques.

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