A study of High Voltage Oxide Breakdown Voltage Drop induced by Etch Damage in NAND Flash Memory

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In NAND Flash memory, program and erase operation are accomplished by FNT (Fowler-Nordheim Tunneling) scheme in order to write the desired data in memory cells. For FN tunneling, the electric field of ~20V level has to be applied to the memory cells, and the electric field of the cells is provided from the HV transistor after generating the high voltage of ~27V level in the pump circuit. Therefore, the BV (Breakdown Voltage) characteristic of HV transistor is important in the NAND flash memory. But recently, the transistor size of the peripheral circuit is reduced along with the cell size reduction for high density & speed. The reduction of peripheral circuit size makes the reliability of HV transistor to be weaker. Recently, the oxide burst failure occured in the Sub-20nm NAND flash memory. In wafer level test, this failure is not screened and it appears in the bathtub test or the package level evaluation, and HV oxide BV drop phenomenon appears simultaneously. Figure 1 shows HVE oxide burst defect with the analysis image in the package test. The defect location is the HVE transistor pattern intermediate area from gate direction, and is the STI (Shallow Trench Isolation) field edge area which the electric field is concentrated in HVE transistor positive sweep operation. The simulation of figure 2 shows the electric field of the STI area during HVE transistor operation. Figure 2 shows the electric field intensity of the active field edge area in positive sweep. As shown in the Figure 2, the electric field is concentrated on active field edge area, and this can be confirmed with the vertical direction between silicon substrate and F-Poly (Floating Poly). As a result, we could know that the electric field intensity of the active field edge area makes the HVE oxide burst defect and BV drop. Accordingly, we made the HV oxide BV output factor, and we should improve the process in order to raise HV oxide BV level. Firstly, there is a simple way. HV oxide BV can be improved by raising oxide thickness. But we cannot use this method, because it changes not only BV but also the device characterization including the operation voltage, device speed, and etc. Therefore, we should find the root cause and improve the process for eliminating the reliability failure.

We investigated oxide burst of HVE (High Voltage Enhancement) transistor of Sub-20nm NAND Flash memory in reliability evaluation, and oxide burst was shown to be related to HV oxide BV (Breakdown Voltage) drop. HV oxide BV can be improved by changing oxide thickness. However, this method changes not only HV oxide BV but also device characterization. So, we should find another method. This paper presents the detail studies of HV transistor BV characteristics that have been carried out to optimize the peripheral circuit area active trench etch condition.

We have discussed about HVE transistor failure issue in bathtub and package level evaluation. We made the HV oxide BV output factor, because the electric field concentration of the active field edge area made the HV oxide burst and BV drop.