A novel Vertical-cell transistor DRAM to suppress the floating body effect by Buried-body Diode Structure (BDS)

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It is verydifficult to maintain the existing DRAM structure in order to sharply reducethe chip size. Recently, we are actively studying the relationship between theDRAM structure and the chip size. One of these is a vertical cell DRAM, whichhas the advantage of reducing chip area by about 1/3 compared to conventionalcell DRAM. However, since the bit line is made in Si trenches, it can cause afloating-body effect, which increases off-current. Here, we suggest the Buriedbody Diode Structure (BDS) as a simple way to deal with these disadvantageswithout changing the materials. In the new structure, a tunnel diode bodycontact is embedded in the source region, which can effectively release theaccumulated body carriers. In a cell transistor, a heavily doped p+ layer isintroduced beneath the n+ source region so that the body and the source areeffectively connected through tunneling. The holes caused by floating body effect flow tothe p+ region and are then released by tunneling. Both p+ and n+ region in thisdiode were attenuated, where the Fermi levels were set inside the valence bandof the p+ region or the conduction band of the n+ source. The new structure does not enlarge the device size and suppress the floatingbody effect.