# 41G. TCAD for Nano-Scale FET

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<th>Session Date:</th>
<th>March 9(Thu.), 2023</th>
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<td>Session Time:</td>
<td>14:45-16:10</td>
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<td>Session Room:</td>
<td>Room G (#318)</td>
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<td>Session Chair:</td>
<td>Prof. Rock-Hyun Baek (Pohang University of Science and Technology)</td>
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</tbody>
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## [41G-1] [Invited] Deep Learning for Semiconductor Materials and Devices Design

Changwook Jeong\textsuperscript{1}, Sanghoon Myung\textsuperscript{2}, Byungseon Choi\textsuperscript{2}, Jinwoo Kim\textsuperscript{2}, Wonik Jang\textsuperscript{2}, In Huh\textsuperscript{2}, Jae Myung Choe\textsuperscript{2}, Young-Gu Kim\textsuperscript{2} and Dae Sin Kim\textsuperscript{2}

\textsuperscript{1}Ulsan National Institute of Science and Technology, \textsuperscript{2}Samsung Electronics Co., Ltd.

## [41G-2] Optimization of Ge Mole Fraction in Sacrificial Layers for Sub-3-nm Node Silicon Nanosheet FETs

Sanguk Lee, Jinsu Jeong, Jun-Sik Yoon, Seunghwan Lee, Junjong Lee, Jaewan Lim and Rock-Hyun Baek

Pohang University of Science and Technology

## [41G-3] Investigation of Self-Heating Effect in Forksheet FETs for Sub-3-nm Node

Jaewan Lim, Jinsu Jeong, Junjong Lee, Seunghwan Lee, Sanguk Lee and Rock-Hyun Baek

Pohang University of Science and Technology

## [41G-4] Process Condition Effects on Saddle Fin Profile and Its Device Performance below 20nm Advanced DRAM

Yexiao Yu, Zhongming Liu and Hong Ma

ChangXin Memory Technologies, Inc.

## [41G-5] Process-Induced Uniaxial Strain in Nanosheet-FET Based CMOS Technology – Is It Still Beneficial?

Ramandeep Kaur and Nihar R. Mohapatra

Indian Institute of Technology Gandhinagar