

## 7<sup>th</sup> IEEE Electron Devices Technology and Manufacturing (EDTM) Conference 2023

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48G. Modeling for Variability and Manufacturing	
Session Date:	March 9(Thu.), 2023
Session Time:	16:30-17:55
Session Room:	Room G (#318)
Session Chair	Prof. Jong-Ho Bae (Kookmin University)

[48G-1] [Invited] 16:30-16:55

## Advanced Compact Modeling for Transistor Aging: Trap-Based Approaches and Mixed-Mode Coupling

Runsheng Wang<sup>1</sup>, Zixuan Sun<sup>1</sup>, Yu Li<sup>1</sup>, Yongkang Xue<sup>2</sup>, Zirui Wang<sup>1</sup>, Pengpeng Ren<sup>2</sup>, Zhigang Ji<sup>1,2</sup>, Lining Zhang<sup>1</sup> and Ru Huang<sup>1</sup>

<sup>1</sup>Peking University, <sup>2</sup>Shanghai Jiao Tong University

[48G-2] 16:55-17:10

## Integrated Wafer and Die Level Simulation of Back End of Line Chemical Mechanical Polishing Processes

Ushasree Katakamsetty<sup>1</sup>, Stefan Nikolaev Voykov<sup>2</sup>, Boris Vasilev<sup>3</sup>, Sam Nakagawa<sup>4</sup>, Tamba Tugbawa<sup>5</sup>, Jansen Chee<sup>6</sup>, Aaron Gower-Hall<sup>7</sup>, Brian Lee<sup>7</sup>, Weiyang Zhu<sup>8</sup>, Bifeng Li<sup>8</sup> and Kimiko Ichikawa<sup>9</sup>

<sup>1</sup>Global Foundries, Singapore, <sup>2</sup>Global Foundries, Sofia, Bulgaria, <sup>3</sup>Global Foundries, Dresden, Germany, <sup>4</sup>Global Foundries, Santa Clara, CA, <sup>5</sup>Cadence Design Systems, Inc., San Jose, CA, USA, <sup>6</sup>Cadence Design Systems, Inc., Singapore, <sup>7</sup>Cadence Design Systems, Inc., Burlington, MA, USA, <sup>8</sup>Cadence Design Systems, Inc., Yokohama, Japan [48G-3]

Introduction and Research of All Wafer Intelligent Monitoring (AIM) System

Junho Roh, Jinil Kim, Hong-Goo Lee, Sang-Ho Lee and Jaewook Seo *SK hynix Inc.* 

[48G-4] 17:25-17:40

## Drain Current Variability in 2-Levels Stacked Nanowire Gate All Around P-Type Field Effect Transistors

Donghyun Kim<sup>1,2</sup>, Sylvain Barraud<sup>3</sup>, Gerard Ghibaudo<sup>1</sup>, Christoforos Theodorou<sup>1</sup> and Jae Woo Lee<sup>2</sup> <sup>1</sup>Univ. Grenoble Alpes, Univ. Savoie Mont Blanc, Grenoble INP, CNRS, IMEP-LAHC, <sup>2</sup>Korea University, <sup>3</sup>Université Grenoble Alpes CEA-Leti

[48G-5] 17:40-17:55

Application of Deep Artificial Neural Network to Model Characteristic Fluctuation of Multi-Channel Gate-All-Around Silicon Nanosheet and Nanofin MOSFETs Induced by Random Nanosized Metal Grains

Sagarika Dash, Yiming Li and Wen-Li Sung National Yang Ming Chiao Tung University